Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A pixel structure formed on a transparent substrate, comprising:
a first conductive layer formed on a transparent substrate, wherein the first conductive layer comprises a scan line and a gate,- the gate and the scan line being electrically connected together;
a first dielectric layer formed on the transparent substrate covering the first conductive layer;
a channel layer formed over the first dielectric layer above the gate;
a second conductive layer formed over the first dielectric layer, wherein the second conductive layer comprises a data line and a source/drain such that the gate, the channel layer and the source/drain together constitute a thin film transistor, and the data line in the area above the scan line branches out into a plurality of subsidiary lines;
a second dielectric layer formed on the first dielectric layer covering the second conductive layer; and
a pixel electrode formed over the second dielectric layer, wherein the pixel electrode, the data line and the source/drain are electrically connected together.

[c2] 2. The pixel structure of claim 1, wherein the width of the scan line in the area underneath the data line is smaller than the width of the scan line in other areas.

[c3] 3. The pixel structure of claim 1, wherein the second dielectric layer furthermore comprises a contact opening such that the pixel electrode and the source/drain are electrically connected through a contact inside the contact opening.

[c4] 4. The pixel structure of claim 1, wherein material constituting the pixel electrode is selected from a group consisting of indium-tin oxide and indium-zinc oxide.

[c5] 5. A pixel structure formed on a transparent substrate, comprising:
a first conductive layer formed on a transparent substrate, wherein the first conductive layer comprises a scan line and a gate, the gate and the scan line being electrically connected together;
a first dielectric layer formed on the transparent substrate covering the first conductive layer;
a channel layer formed over the first dielectric layer above the gate;
a second conductive layer formed over the first dielectric layer, wherein the second conductive layer comprises a

data line, a repair line and a source/drain such that the gate, the channel layer and the source/drain together constitute a thin film transistor, and the repair line is positioned on one side of the data line with a portion of the repair line crossing over the scan line;
a second dielectric layer formed on the first dielectric layer covering the second conductive layer; and
a pixel electrode formed over the second dielectric layer, wherein the pixel electrode, the data line and the source/drain are electrically connected together.

[c6] 6. The pixel structure of claim 5, wherein the repair line furthermore comprises a first end and a second end such that the first end of the repair line and the data line are electrically connected but the second end of the repair line has no electrical connection with the data line.

[c7] 7. The pixel structure of claim 5, wherein the repair line furthermore comprises a first end and a second end such that both the first end and the second end have no electrical connection with the data line.

[c8] 8. The pixel structure of claim 5, wherein the second dielectric layer has a contact opening such that the pixel electrode and the source/drain are electrically connected through a contact inside the contact opening.

[c9] 9. The pixel structure of claim 5, wherein material constituting the pixel electrode is selected from a group consisting of indium-tin oxide and indium-zinc oxide.

[c10] 10. A pixel structure comprising a scan line, a data line, a pixel electrode and a thin film transistor, wherein the thin film transistor comprises a gate, a channel layer and a source/drain such that the gate and the scan line are electrically connected and the source/drain, the data line and the pixel electrode are electrically connected, and one major characteristic of the pixel structure is that the data line in area above the scan line branches out into a plurality of subsidiary lines.

[c11] 11. The pixel structure of claim 10, wherein the width of the scan line in the area underneath the data line is smaller than the width of the scan line in other areas.

[c12] 12. A pixel structure comprising a scan line, a data line, a pixel electrode and a thin film transistor, wherein the thin film transistor comprises a gate, a channel layer and a source/drain such that the gate and the scan line are electrically connected and the source/drain, the data line and the pixel electrode are electrically connected, and one major characteristic of the pixel structure is that a repair line is set up on one side of the data line with a portion of the repair line crossing over the scan line.

[c13] 13. The pixel structure of claim 12, wherein the repair line furthermore comprises a first end and a second end such that the first end of the repair line connects with the data line but the second end of the repair line has no electrical connection with the data line.

[c14] 14. The pixel structure of claim 12, wherein the repair line furthermore comprises a first end and a second end such that both the first end and the second end have no electrical connection with the data line.